IN THE SPECIFICATION:

Please substitute the following paragraph for the paragraph starting at page 6, line 15 and ending at page 7, line 1.

It is an object of the present invention to realize a configuration capable of preferably carrying out image display using a modulation side drive circuit including a conversion circuit (shift register and the like) for converting a time-series signal to a parallel signal. More specifically, it is one of the objects of the present invention to provide an image display apparatus that can manage with a low operating speed of a conversion circuit and/or a small memory usage, an image display method for the image display apparatus, an image display program for the image display method and a computer readable recording medium having the image display program recorded therein.

Please substitute the following paragraph for the paragraph starting at page 17, line 23 and ending at page 18, line 11.

In addition, according to a further ~~another~~ aspect of the present invention, a configuration can be preferably employed in which the input signal to be inputted in the above-mentioned output circuit in time-series in order to output the above-mentioned plurality of parallel outputs is n time-series input signals for generating n modulation signals to be supplied to the above-mentioned modulation wirings in parallel, the above-mentioned output circuit is for storing the n time-series input signals in first to Dth memories (D is an integer equal to or larger than 3) one after another in the order of input, and the above-mentioned each memory is for writing the input signals in an address to be designated by a write address to be given and reading a signal written in an address designated by a read address to be given,

Please substitute the following paragraph for the paragraph starting at page 41, line 17 and ending at line 19.

In addition, the timing controller 34 can also be implemented in a logic circuit (ASIC and the like) by [[a]] hardware.

Please substitute the following paragraph for the paragraph starting at page 46, line 7 and ending at page 47, line 3.

Here, an output circuit having a plurality of output paths (each of which is connected to each modulation side drive circuit, in particular, to a shift register) as the output circuit (multi-layered buffer 32) (more specifically, a configuration having a plurality of memories including output ports connected to the above-mentioned output paths) is employed, whereby modulated data can be outputted to a plurality of modulation side drive ~~circuit~~ circuits in parallel with each other. In particular, the circuit is structured such that modulated data for one scan wiring to be inputted in the output circuit (multi-layered buffer 32) in time-series is divided into each part corresponding to each modulation side drive circuit and each part is outputted to each output path. That is, modulated data (n input signals) for one scan wiring is divided into D pieces and outputted as D outputs. Here, an Xth ($1 \leq X \leq D$) output is constituted by signals for generating a modulation signal to be supplied to a plurality of modulation wirings to be connected to a modulation side drive circuit corresponding to the Xth output. In addition, the following conditions are employed in outputting modulated data for one scan wiring.

Please substitute the following paragraph for the paragraph starting at page 47, line 26 and ending at page 48, line 3.

By satisfying these conditions, a configuration can be realized which is capable of lowering a communication rate (transfer rate) of modulated data from the output circuit to the modulation side drive circuit with [[a]] less storage capacity.

Please substitute the following paragraph for the paragraph starting at page 61, line 27 and ending at page 62, line 6.

Reference numerals 741, 742 and 743 denote a first memory, a second memory and a third memory, respectively. The memory A 741 has a capacity that is one fifth of the capacity for one scan wiring, and the memory B 742 and the memory C 743 have capacities that are two-fifths ~~fifth~~ of the capacity for one scan wiring, respectively.

Please substitute the following paragraph for the paragraph starting at page 63, line 8 and ending at line 12.

By giving the above-mentioned control signals, data of 1 to n/5 of the luminance signal S3 is outputted to the memory A read data S71 at a speed that is two-fifths ~~fifth~~ of the data speed of the luminance signal S3, with the delay of 3/5 scanning period.

Please substitute the following paragraph for the paragraph starting at page 63, line 13 and ending at line 17.

Similarly, data of n/5+1 to 3n/5 of the luminance signal S3 is outputted to the memory B read data S72 at a speed that is ~~two fifth~~ two-fifths of the data speed of the luminance signal S3, with the delay of 3/5 scanning period.

Please substitute the following paragraph for the paragraph starting at page 63, line 18 and ending at line 22.

Similarly, data of n/5+1 to n of the luminance signal S3 is outputted to the memory C read data S73 at a speed that is ~~two-fifth~~ two-fifths of the data speed of the luminance signal S3, with the delay of 3/5 scanning period.

Please substitute the following paragraph for the paragraph starting at page 63, line 23 and ending at page 64, line 2.

Consequently, it can be realized to transfer data in parallel with each other to the shift register divided into three blocks and to reduce the transfer speed of the transfer data S31 to S33 and the operation speed of the shift register to ~~two-fifth~~ two-fifths, using a memory capacity equal to the capacity for one scanning wiring.

Please substitute the following paragraph for the paragraph starting at page 83, line 23 and ending at page 84, line 8.

In the above-mentioned embodiments, data corresponding to a plurality of colors (R, G and B) is divided by driving display elements such that data arranged in time-series in advance is transmitted in parallel with each other to a plurality of modulation side drive ~~circuit~~ circuits. However, an embodiment of the present invention is not limited to this. In an eighth embodiment, a configuration will be described in which modulated data for each color is divided separately, and[[,]] then[[,]] data corresponding to a plurality of colors that are composed and arranged in time-series are used in a modulation side drive circuit.